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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/783,195	02/20/2004	Mou-Shiung Lin	MS98-002CCC CIPB	6169

7590 07/05/2005

George O. Saile
28 Davis Avenue
Poughkeepsie, NY 12603

EXAMINER	
LE, THAO X	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 07/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/783,195	LIN ET AL.	
	Examiner	Art Unit	
	Thao X. Le	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *94-131* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *94-131* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/29/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Acknowledgement

1. Applicant's cancellation of claims 1-93 in the amendment file on 06/15/05 is acknowledged.

Drawings

2. The drawings were received on 15 June 2005. These drawings are acceptable.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 95-96, 107-108, 126-127 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The specification discloses the passivation layer 4 in fig. 2 comprises oxide and nitride. But it fails to disclose layer 4 is the TOPMOST oxide or nitride layer as claimed in claims 95-96, 107-108, and 126-127. Thus, they are indefinite.

For the purpose of examination, the passivation layer is being interpreted as comprises a nitride or oxide layer.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 94-98, 101-102, and 104 are rejected under 35 U.S.C. 102(b) as being anticipated by US 5659201 to Wollesen.

Regarding claim 94, Wollesen discloses a semiconductor chip or wafer in fig. 7 comprising: a semiconductor substrate 1, fig 1 column 1 line 53 and column 6 line 56, having multiple semiconductor devices, fig. 1, an interconnecting metallization structure 20/22/28, column 6 lines 52 and 55, over said semiconductor substrate 1; a passivation layer 23/24, fig. 7 column 6 lines 57-59, over said interconnecting metallization structure 20/22/28; and an upper metallization structure 71, column 8 line 22, over said passivation layer 24/24 and comprising gold, column 5 line 17, wherein said upper metallization structure 71 comprises a connecting portion 72 connecting multiple portions of said interconnecting metallization structure 20/22/28, fig. 7.

Regarding claims 95-96, Wollesen discloses the semiconductor chip or wafer of claim 94, wherein said passivation layer 23/24 comprises a nitride layer 24, column 6 lines 59 and oxide layer 23, column 6 line 60 of said semiconductor chip or wafer.

Regarding claim 97, Wollesen discloses the semiconductor chip or wafer of claim 94, wherein said passivation layer comprises a topmost insulation layer 70, column 8

line 28, formed using a CVD process, column 6 line 47, of said semiconductor chip or wafer.

Regarding claim 98, Wollesen discloses the semiconductor chip or wafer of claim 94, wherein said interconnecting metallization structure comprises a first contact pad (right portion of 71) exposed by an opening in said passivation layer 23/24, and said upper metallization structure 71 comprises a second contact pad (left portion of 71) connected to said first contact pad, wherein the positions of said first and second contact pads from a top view are different, fig. 7.

Regarding claim 101, Wollesen discloses the semiconductor chip or wafer of claim 94, wherein said semiconductor substrate 1 comprises silicon, column 1 line 53 (semiconductor comprises silicon).

Regarding claim 102, Wollesen discloses the semiconductor chip or wafer of claim 94 further comprising a topmost polymer 70 layer over said passivation layer 23/24, wherein said upper metallization structure comprises an upper metal layer 71 over said topmost polymer layer 70.

Regarding claim 104, Wollesen discloses the semiconductor chip or wafer of claim 94, wherein said interconnecting metallization structure 20/22/28 comprises aluminum, column 6 line 54.

7. Claims 103, 105 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over US 5659201 to Wollesen.

Regarding claims 103 and 105, Wollesen discloses the semiconductor chip or wafer of claim 94, wherein said interconnecting metallization structure 20/22/28

comprises copper, column 6 line 61, wherein said upper metallization 71 structure comprises a metal, column 8 line 23.

The process limitations to 'electroplated copper' or 'electroplated metal' in claims 103 and 105 do not carry weight in a claim drawn to structure. In re Thorpe, 277 USPQ 964 (Fed. Cir. 1985).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

10. Claims 99-100, 106-131 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5659201 to Wollesen.

Regarding claim 99, Wollesen discloses the semiconductor chip or wafer of claim 94, wherein said gold comprises a gold layer 7, column 5 line 17.

But, Wollesen does not disclose the gold layer 71 having a thickness of between 2 and 100 μm.

However, Wollesen discloses the gold layer 71 having a general thickness. Accordingly, it would have been obvious to one of ordinary skill in art to use or combine (teaching of second reference) in the range as claimed, because it has been held that where the general conditions of the claims are discloses in the prior art, it is not inventive to discover the optimum or workable range by routine experimentation. See In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). Furthermore, the thickness of bonding pad in the range of 2 and 100 μm are typical as disclosed by Chen (6001538) in column 3 line 53-55 or Sebesta (6900545) in abstract.

Regarding claims 100, 110 Wollesen discloses the semiconductor chip or wafer of claim 99, wherein said upper metallization structure further comprises a metal layer 73, column 8 line 21, under said gold layer 71, wherein said metal layer 73 comprises titanium tungsten, column 5 line 43.

Regarding claim 106, Wollesen discloses a semiconductor chip or wafer in fig. 7 comprising: a semiconductor substrate 1, fig 1 column 1 line 53 and column 6 line 56, having multiple semiconductor devices, fig. 1, an interconnecting metallization structure 20/22/28, column 6 lines 52 and 55, over said semiconductor substrate 1 and comprising a first contact pad (right portion of 71), fig. 7; a passivation layer 23/24, fig. 7

column 6 lines 57-59, over said interconnecting metallization structure 20/22/28, wherein said first contact pad is exposed by an opening in said passivation layer 23/24; and an upper metallization structure 71, column 8 line 22, over said passivation layer 24/24 and comprising gold, column 5 line 17, wherein said upper metallization structure 71 comprises a second contact pad (left portion of 71), fig. 7, connected to said first contact pad, and wherein the positions of said first and second contact pads from a top view are different, fig. 7.

But, Wollesen does not disclose the gold layer 71 having a thickness of between 2 and 100 μm.

However, Wollesen discloses the gold layer 71 having a general thickness. Accordingly, it would have been obvious to one of ordinary skill in art to use or combine (teaching of second reference) in the range as claimed, because it has been held that where the general conditions of the claims are discloses in the prior art, it is not inventive to discover the optimum or workable range by routine experimentation. See In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). Furthermore, the thickness of bonding pad in the range of 2 and 100 μm are typical as disclosed by Chen (6001538) in column 3 line 53-55 or Sebesta (6900545) in abstract.

Regarding claims 107-108, 126-127, Wollesen discloses the semiconductor chip or wafer of claim 94, wherein said passivation layer 23/24 comprises a nitride layer 24, column 6 lines 59 and oxide layer 23, column 6 line 60 of said semiconductor chip or wafer.

Regarding claim 109, 128, Wollesen discloses the semiconductor chip or wafer of claim 94, wherein said passivation layer comprises a topmost insulation layer 70, column 8 line 28, formed using a CVD process, column 6 line 47, of said semiconductor chip or wafer.

Regarding claim 111, Wollesen discloses the semiconductor chip or wafer of claim 94, wherein said semiconductor substrate 1 comprises silicon, column 1 line 53 (semiconductor comprises silicon).

Regarding claim 112-115, Wollesen does not disclose the semiconductor chip or wafer of claim 106 further comprising a wire bonded connected to said second contact pad, and further comprising a metal bump formed on said second contact pad.

However, Wollesen discloses in fig. 1 a second contact pad 14, column 2 line 14, comprising a wire bonded 15 connected to said second contact pad 14, and further comprising a metal bump (bottom portion of wire 15) formed on said second contact pad. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use wire and metal bump teaching of Wollesen as claimed, because it would have allowed the external electrical connection.

Regarding claim 116, 123, Wollesen discloses the semiconductor chip or wafer of claim 94 further comprising a topmost polymer 70 layer over said passivation layer 23/24, wherein said upper metallization structure comprises an upper metal layer 71 over said topmost polymer layer 70.

Regarding claims 117, 119, Wollesen discloses the semiconductor chip or wafer of claim 94, wherein said interconnecting metallization structure 20/22/28 comprises copper, column 6 line 61, wherein said upper metallization 71 structure comprises a metal, column 8 line 23.

The process limitations to 'electroplated copper' or 'electroplating ' in claims 117 and 119 do not carry weight in a claim drawn to structure. In re Thorpe, 277 USPQ 964 (Fed. Cir. 1985).

Regarding claim 118, Wollesen discloses the semiconductor chip or wafer of claim 94, wherein said interconnecting metallization structure 20/22/28 comprises aluminum, column 6 line 54.

Regarding claims 120, Wollesen discloses a semiconductor chip or wafer in fig. 7 comprising: a semiconductor substrate 1, fig 1 column 1 line 53 and column 6 line 56, having multiple semiconductor devices, fig. 1, an interconnecting metallization structure 20/22/28, column 6 lines 52 and 55, over said semiconductor substrate 1 and comprising a contact point 72, fig. 7 column 8 line 19, a passivation layer 23/24, fig. 7 column 6 lines 57-59, over said interconnecting metallization structure 20/22/28, wherein said first contact point 72 is exposed by an opening in said passivation layer 23/24; and an upper metallization structure 71, column 8 line 22, over said contact point 72, wherein said upper metallization structure 71 comprises a contact pad, fig. 7, comprising gold layer, column 5 line 17, and connecting to contact point 72.

But, Wollesen does not disclose the gold layer 71 having a thickness of between 2 and 100 μm, and wherein said contact pad is used to be wirebonded thereto or has a metal bump formed thereon.

However, Wollesen discloses the gold layer 71 having a general thickness. Accordingly, it would have been obvious to one of ordinary skill in art to use or combine (teaching of second reference) in the range as claimed, because it has been held that where the general conditions of the claims are discloses in the prior art, it is not inventive to discover the optimum or workable range by routine experimentation. See In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). Furthermore, the thickness of bonding pad in the range of 2 and 100 μm are typical as disclosed by Chen (6001538) in column 3 line 53-55 or Sebesta (6900545) in abstract.

With respect to wirebonded and metal bump, Wollesen discloses in fig. 1 and 6 a second contact pad 14, column 2 line 14, comprising a wire bonded 15 connected to said second contact pad 14, and further comprising a metal bump (bottom portion of wire 15) formed on said second contact pad. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use wire and metal bump teaching of Wollesen as claimed, because it would have allowed the external electrical connection.

Regarding claims 121-122, 124-125, 129, Wollesen discloses the semiconductor chip or wafer of claim 120, wherein said contact point comprises aluminum, 8 line 20 or copper, column 8 line 25, and having gold layer 71, column 5 line 17.

The process limitations to 'electroplated copper' in claims 122, 124 and 'electroplating' in claim 129 do not carry weight in a claim drawn to structure. In re Thorpe, 277 USPQ 964 (Fed. Cir. 1985).

Regarding claim 130-131, Wollesen does not disclose the semiconductor chip or wafer of claim 120, wherein said metal bump comprises solder, and further comprising a wirebonded connected to said contact pad.

However, Wollesen discloses in fig. 1 a second contact pad 14, column 2 line 14, comprising a wire bonded 15 connected to said second contact pad 14, and further comprising a metal bump (bottom portion of wire 15) formed on said second contact pad. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use wire and metal bump teaching of Wollesen as claimed, because it would have allowed the external electrical connection.

With respect 'solder', the wirebonded connection as disclosed by Wollesen in fig. 1 would include solder, because solder is an integral part of the wire boning process.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X. Le whose telephone number is (571) 272-1708. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on (571) 272 -1705. The fax phone

number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thao X. Le
Patent Examiner
28 June 2005

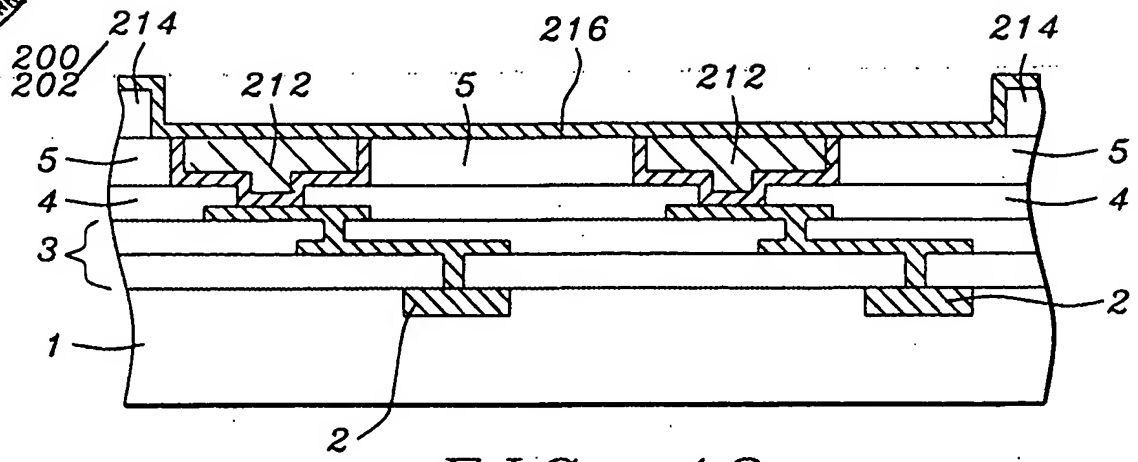

FIG. 18

OK
TL

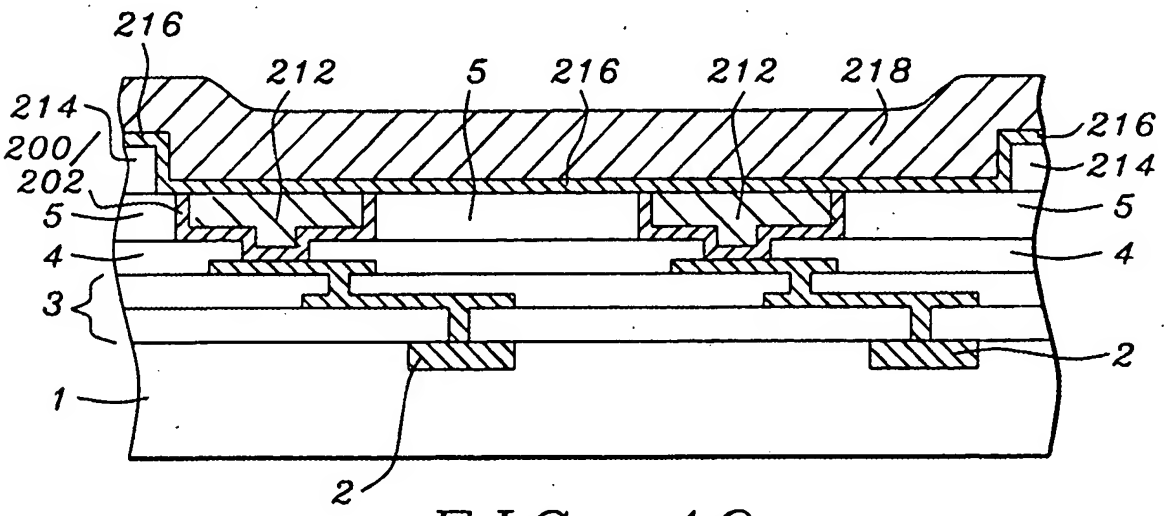

FIG. 19

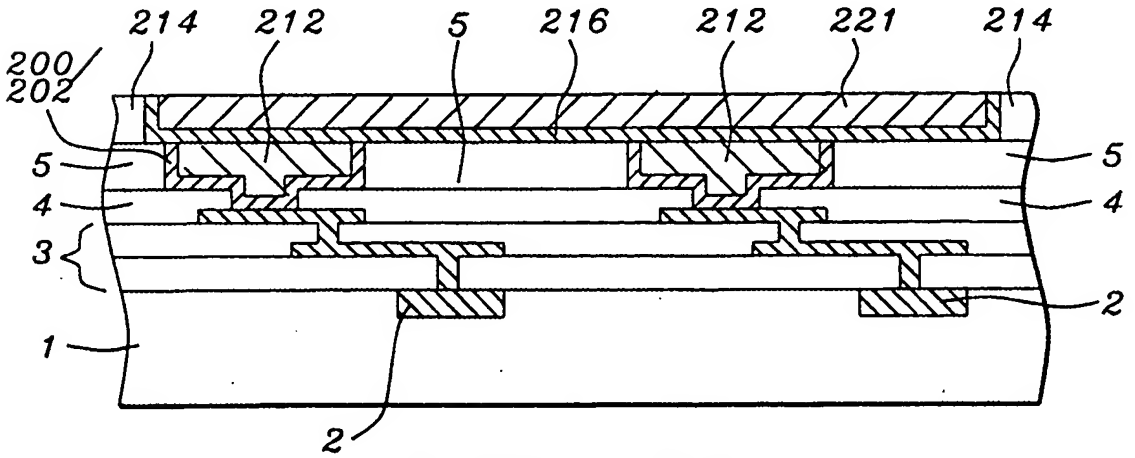

FIG. 20

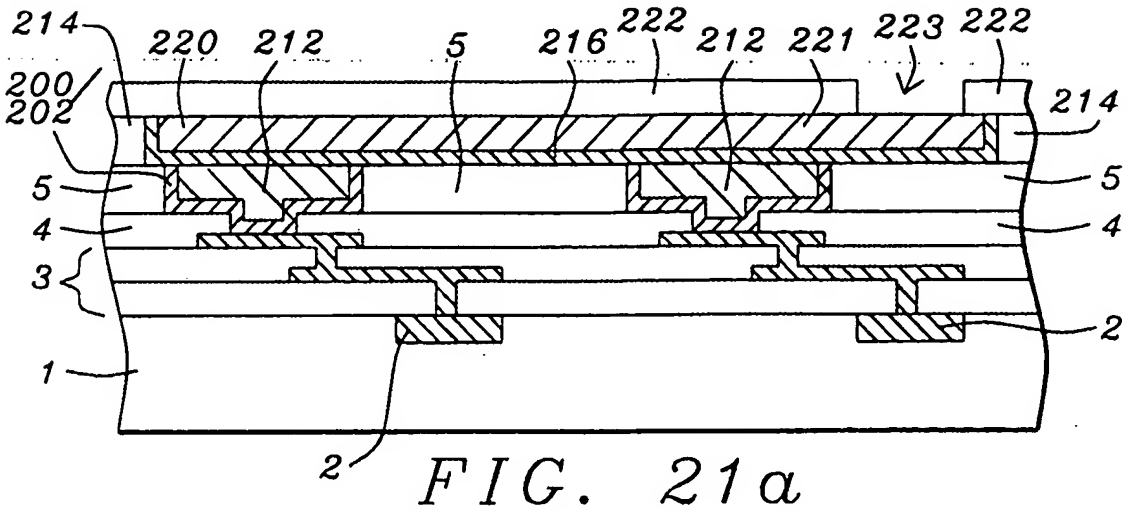

FIG. 21a

ok
TR

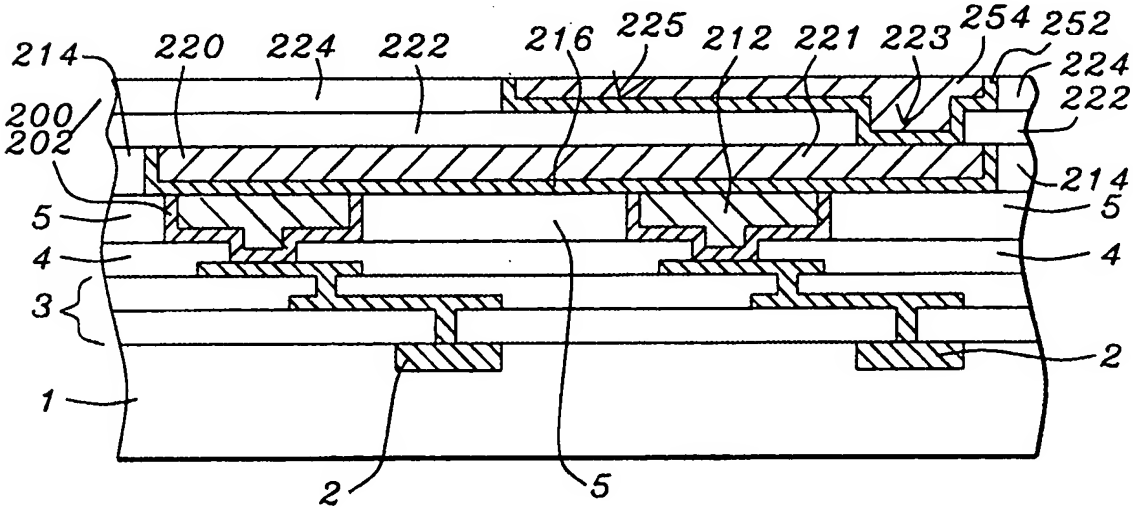

FIG. 21b

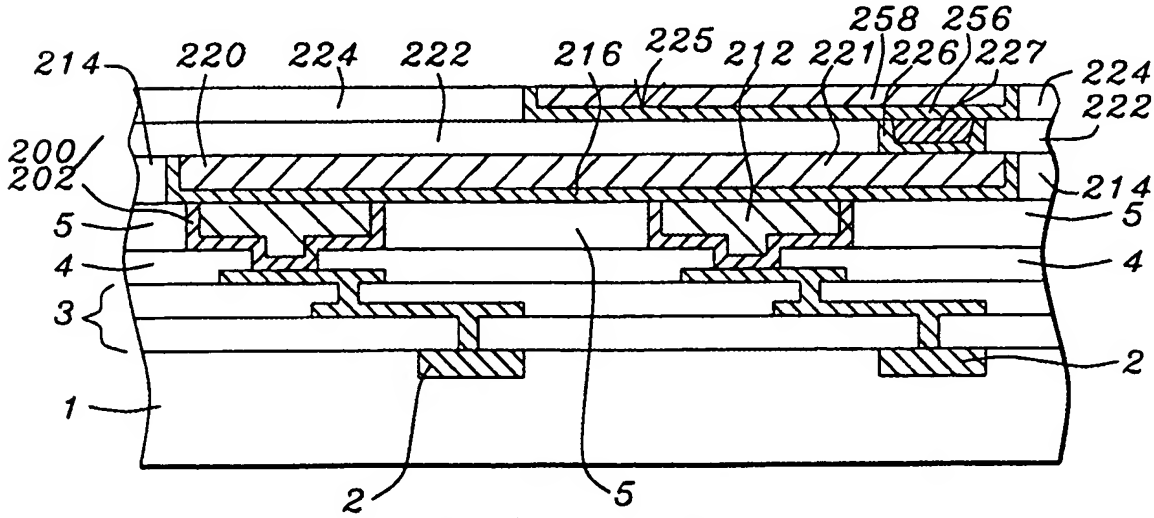

FIG. 21c